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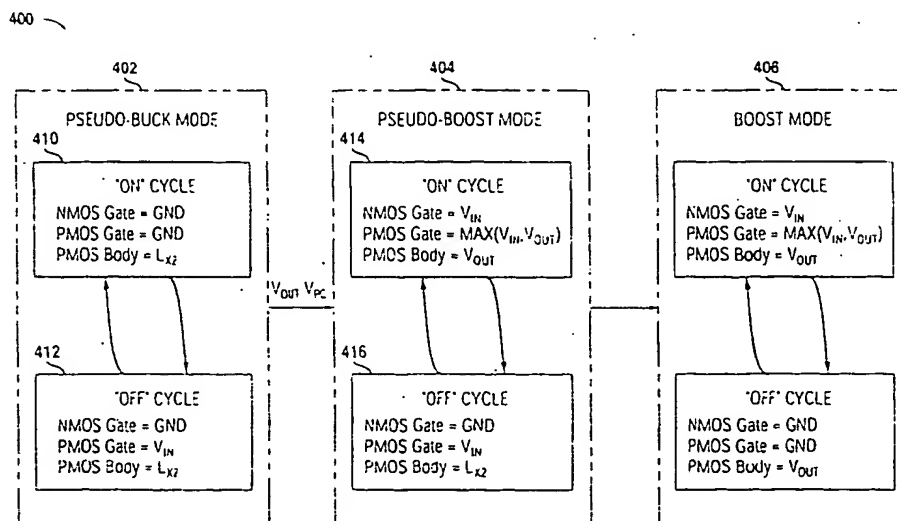
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(54) Title: SWITCHING POWER SUPPLIES WITH LINEAR PRECHARGE, PSEUDO-BUCK AND PSEUDO-BOOST MODES

(57) Abstract

The present invention teaches a variety of startup modes for operating a boost type switching power supply. A linear charging mode couples the input voltage directly to the output voltage, thereby precharging the output capacitor of the switching power supply. The linear mode serves to reduce inrush battery current and limit the stress voltage on the power switching devices. A pseudo-buck mode (402), preferably entered into after the linear mode has precharged the output capacitor, operates the boost type switching power supply in a manner providing power to the output essentially as a buck type switching power supply would. This results in continuous charging of the output capacitor, thereby reducing startup time and increasing power efficiency. The pseudo-buck mode (402) also enables step-down voltage generation with boost type circuitry. A pseudo-boost mode (404) facilitates a smooth transition between the pseudo-buck and traditional boost modes.

SWITCHING POWER SUPPLIES WITH LINEAR PRECHARGE,
PSEUDO-BUCK AND PSEUDO-BOOST MODES

Description

Technical Field

The present invention is related to DC to DC switching power supplies, particularly those having boost type circuit topology. More specifically, the present invention teaches three different operating modes for a boost type circuit that together provide control over the inductor inrush current, as well as allowing the use of smaller power devices by limiting the operating

10   voltage seen by the power devices.

Background Art

Switching power supplies are known in the art. Typical uses of switching power supplies include generating a constant, regulated output voltage Vout from an input source, whose voltage

15   Vin may be decreasing in amplitude over time. A switching power supply having a "boost" circuit topology is capable of generating a regulated output voltage Vout that is greater than the unregulated supply voltage Vin. As an example, a switching power supply may be used to generate a regulated output voltage Vout from the potential difference across terminals of a battery in order to operate an electrical device such as a portable computer, a radio, a CD player,

20   a cellular phone or the like. As the electrical device drains energy from the battery, the input voltage Vin supplied by the battery diminishes over time, and it is the job of the boost regulator to continue generating a constant output voltage Vout to keep the electrical device operating.

With reference to Figures 1-2, the topography and operation of a traditional boost switching regulator 100 of the Prior Art will now be described. Prior Art Figure 1 illustrates the

25   boost switching regulator 100 including an inductor L, an output filter capacitor C, an n-channel Metal-Oxide Semiconductor Field Effect Transistor (NMOS) switch 102, a p-channel MOSFET (PMOS) switch 104, and duty-cycle control circuitry 106. Voltage Vin is typically an unregulated source of DC voltage connected to a first terminal of the inductor L and to a common ground reference 110. The second terminal of the inductor L and the drains of the

30   switches 102 and 104 are coupled together at a node Lx. The source and body of the PMOS switch 104 are coupled together at a first terminal of the capacitor C, thereby forming a PMOS body diode from Lx to the first capacitor terminal. The control circuitry 106 implements a duty-cycle algorithm, controlling the operation of the NMOS switch 102 and the PMOS switch 104.

The second terminal of the capacitor C, a second terminal of the voltage Vin, and the source and body of the NMOS switch 102 are all coupled to a common ground reference 110. The output voltage Vout of the switching regulator 100 measured across the output capacitor C.

Prior Art Figure 2 illustrates a state diagram 150 for operation of the boost switching regulator 100. During an on-cycle 152, the duty-cycle control 106 turns the NMOS switch 102 on and the PMOS switch 104 off. The inductor current Il thus increases at a rate of about Vin/L and, since the PMOS switch 104 is off, no power is transferred from the inductor L to the output. During an off-cycle 154, the duty-cycle control 106 turns the NMOS switch 102 off and the PMOS switch 104 on. Hence during the off-cycle 154, power is transferred from the inductor L to the output and the inductor current Il decreases at a rate of (Vout-Vin)/L. For ease of reference, the relevant control voltages for the on-cycle 152 and the off-cycle 154 are shown in both Figure 2 and in the following table.

Traditional Boost	NMOS Gate Drive	PMOS Gate Drive	PMOS Body
On-Cycle 152	Vin	Max(Vin,Vout)	Vout
Off-Cycle 154	Ground	Ground	Vout

As will be appreciated, a variety of duty-cycle algorithms can be implemented by the duty-cycle control 106 in order to regulate the output. For example, in a constant ripple, hysteretic converter, the on-cycle 152 is terminated when the inductor current reaches a predetermined maximum value, and the off-cycle 154 is terminated when the inductor current drops below a predetermined minimum value.

Although the traditional boost topology is effective for regulating power under certain circumstances, both the traditional topology and the prior art control algorithms have significant drawbacks. One such drawback is the inability of prior art algorithms to limit inrush current across a variety of input and output voltages. Large inrush currents tend to drastically reduce the life of battery input power supplies. What is needed is a boost switching power supply capable of limiting inductor current at any point regardless of the input and output voltages.

Disclosure of the Invention

In order to achieve the foregoing and in accordance with the present invention, a variety of switching power supplies and methods for controlling the same are disclosed. In particular, the present invention teaches several modes for operating a boost type switching power supply. A linear charging mode couples the input voltage directly to the output voltage, thereby precharging the output capacitor of the switching power supply. The linear mode serves to reduce inrush battery current and limit the stress voltage on the power switching devices. A pseudo-buck mode, preferably entered into after the linear mode has precharged the output capacitor, operates the boost type switching power supply in a manner providing power to the output essentially as would a buck type switching power supply. This results in continuous charging of the output capacitor, thereby reducing startup time and increasing power efficiency. The pseudo-buck mode also enables step-down voltage generation with boost type circuitry. A pseudo-boost mode facilitates a smooth transition between the pseudo-buck and traditional boost modes. The power devices are operated in the pseudo-buck mode such that control over the inductor current is maintained to minimize inrush current.

One specific embodiment of the present invention teaches a switching power supply having an inductor, an output capacitor, first and second variable impedance devices; and a control circuit for controlling the first and second variable impedance devices. The first variable impedance device couples the inductor and the output capacitor terminal together. The second variable impedance device couples the inductor to a common ground reference. The control circuit is operable to implement one or more of a linear mode, a pseudo-buck mode, and a pseudo-boost mode.

The variable impedance devices may be formed from transistor switches such as NMOS and PMOS devices. In such a case, the pseudo-buck mode is implemented having an on-cycle and an off-cycle. During the pseudo-buck mode on-cycle, the second switch gate is coupled to the common ground reference, the first switch gate is coupled to the common ground reference, the diode anode is coupled to Vout, and the diode cathode is coupled to the second inductor terminal. During the pseudo-buck mode off-cycle, the second switch gate is coupled to the common ground reference, the first switch gate is coupled to a voltage suitable to choke the current flowing through the first switch, the diode anode is coupled to Vout, and the diode cathode is coupled to the second inductor terminal.

Another aspect of the present invention teaches a pseudo-boost mode having an on-cycle and an off-cycle. During the pseudo-boost mode on-cycle, the first switch gate is coupled to the greater of Vin and Vout, the second switch gate is coupled to Vin, the diode anode is coupled to

the second inductor terminal, and the diode cathode is coupled to Vout. During the pseudo-boost mode off-cycle, the second switch gate is coupled to a ground reference, the first switch gate is coupled to Vin, the diode anode is coupled to Vout, and the diode cathode is coupled to the second inductor terminal.

5   In certain embodiments of the present invention, the power supply further includes a third variable impedance device such as a transistor switch having a gate, a source, and a drain, the drain being coupled to the first inductor terminal and the source being coupled to Vout. This enables operation of the power supply in a linear mode during which both the first and second switches are disabled and the third switch gate is coupled to Vin, thereby directly coupling the

10   input voltage Vin to the output voltage Vout through the third switch.

        In preferred embodiments, the power supply is initially operated in the linear mode in order to precharge the output capacitor. Once the output capacitor has reached a desired precharge voltage V_{pc}, the power supply is operated in the pseudo-buck mode until Vout reaches a predefined threshold value V_{t1} that is less than Vin. When Vout is between about V_{t1} and V_{t2},

15   V_{t2} being greater than or equal to Vin, the power supply is then operated in the pseudo-boost mode. Once Vout has exceeded about V_{t2}, the power supply is then operated according to a traditional boost duty-cycle algorithm.

Brief Description of the Drawings

Prior Art Figure 1 is a schematic of a traditional boost power supply.

Prior Art Figure 2 illustrates a state diagram for the on- and off-cycles of the traditional boost power supply of Figure 1.

5   Figure 3 is a schematic of a power supply in accordance with one embodiment of the present invention.

Figure 4 illustrates a state diagram for several different modes of operation for the power supply of Figure 3.

Best Modes for Carrying out the Invention

Figure 3 illustrates a regulated switching power supply 300 in accordance with one embodiment of the present invention. The switching power supply 300 includes an inductor L, a capacitor C, two NMOS transistor switches 302 and 304, a PMOS transistor switch 306, and duty-cycle control circuitry 308. An input power supply provides a voltage Vin coupled to both a first terminal of the inductor L and at the drain of the NMOS switch 302, the voltage Vin measured with respect to a common ground reference 310. The source and body of the NMOS transistor 302, and the first terminal of the output filter capacitor C are coupled together forming the output voltage Vout of the power supply 300. The second terminal of the inductor L and the drains of both the NMOS switch 304 and the PMOS switch 306 are coupled together at a node Lx.

Control circuitry 308 is coupled to drive the gates of the transistors 302-306, and further to sense the voltages at an output Vout and a node Lx. The control circuitry 308 implements a duty-cycle algorithm for providing a regulated power supply having a regulated voltage Vout. Control circuitry 308 may be implemented in a microprocessor, programmable logic such as a PLD, PLL, PAL, or any other suitable circuitry. Several different control algorithms according to the present invention are described below.

The present invention contemplates four distinct modes of operation for a boost power supply such as power supply 300 of Figure 3, including three that are intended for implementation during startup as well as a more traditional boost mode. The startup modes are referred to herein as the "linear" mode, the "pseudo-buck" mode and the "pseudo-boost" mode. Figure 4 illustrates a state diagram 400 progressing through a pseudo-buck, pseudo-boost, and boost modes. As will be described below, each of these modes has particular advantages and requirements. Further, in accordance with the present invention, these modes may be used individually or in various combinations with each other and the traditional boost mode.

The linear mode is a preferred control algorithm when the output voltage Vout is less than a predefined precharge voltage Vpc. During linear mode, the input power supply is directly coupled to the output, enabling the output voltage Vout to charge up to the precharge voltage. To accomplish this, the control circuitry 308 disables the NMOS switch 304 and the PMOS switch 306, and turns the NMOS switch 302 fully on.

By directly coupling the input to the output, the linear mode reduces the battery inrush current normally seen across the inductor L during the initial charging of a regulated power supply. In order to implement the linear mode, the power supply 300 requires an additional NMOS switch, i.e., NMOS switch 302, not required in the traditional boost regulator 100 of

Figure 1. However, by precharging the output voltage Vout, the linear mode reduces the stress voltage placed upon the PMOS switch 306, particularly during the pseudo-buck mode described below. Because of this, the power supply 300 can be designed with a smaller, low-voltage PMOS switch 306. Thus even with an additional NMOS switch, there is nonetheless space savings over having to implement a large PMOS switch.

Once the output voltage Vout has charged up to the precharge voltage Vpc, one embodiment of the present invention teaches transitioning into a pseudo-buck mode 402. During the pseudo-buck mode 402, the NMOS switches 302 and 304 are disabled and the body of the PMOS switch 306 is connected to the node Lx. Hence, that portion of the power supply 300 utilized during the pseudo-buck mode 402 has a topology similar to that of a traditional buck power supply. (Essentially, the inductor L and the PMOS switch 306 are "swapped" with respect to the input voltage Vin.) In fact, as will be seen, the operation of the power supply 300 during the pseudo-buck mode 402 results in charging the output in a manner essentially identical to the traditional buck power supply.

During a pseudo-buck on-cycle 410, the PMOS switch 306 is turned on and the inductor current Il increases at the rate of (Vin-Vout)/L. During a pseudo-buck off-cycle 412, the gate of the PMOS switch 306 is coupled to the input voltage Vin so that the inductor current decreases at a rate of Vgs(PMOS)/L. As shown in Figure 3, Vgs(PMOS) is the voltage differential between the gate and the source of the PMOS switch 306 with the inductor current flowing through the PMOS switch 306.

In the off-cycle 412 of the pseudo-buck mode, as in the traditional buck mode, the inductor current Il must still flow through the PMOS switch 306. However, the control circuitry 308 has set the gate of the PMOS switch 306 to Vin. Therefore, in order for current to keep flowing through the PMOS switch 306, the source of the PMOS switch 306 must fly up to at least a couple volts above the gate of the PMOS switch 306. For example, if the input voltage Vin is nominally 5 Volts, then during the off-cycle 412, the PMOS switch 306 source voltage must fly up to about 6-7 Volts to enable the inductor current to continue flowing. Hence, if one were to skip the linear mode and not precharge the output voltage Vout, the pseudo-buck mode 402 would apply about 6-7 Volts across the PMOS switch 306 during the off-cycle. As a result, a high-voltage, space inefficient PMOS switch would be required. However, providing the linear mode is one method for avoiding this large stress voltage. The precharge voltage should thus be set by reference to the breakdown voltage of the PMOS switch 306. Specifically, the precharge voltage Vpc should be greater than (Vin + Vgs(PMOS) - Vbreakdown). The precharge voltage

Vpc should be chosen without forgetting, however, that the larger Vpc is, the more power inefficient the power supply 300 will be.

Because the inductor current Il continuously charges the output capacitor C during the pseudo-buck mode 402, the startup time of the power supply 300 is less that than obtained by many traditional boost regulator startup algorithms. Further, there is an improvement in power efficiency of the power supply 300 during startup. Another advantage over traditional boost algorithms, the pseudo-buck mode 402 actually enables a circuit having a boost topology (i.e., the power supply 300) to provide a step down operation, working like a buck circuit.

For ease of reference, the relevant control voltages for the pseudo-buck mode 402 are shown in Figure 4 and are also provided in the following table.

Pseudo-Buck	NMOS Gate Drive	PMOS Gate Drive	PMOS Body
On-Cycle 410	Ground	Ground	Lx
Off-Cycle 412	Ground	Vin	Lx

As Vout approaches Vin during the pseudo-buck mode 402, the duty-cycle of the PMOS switch 306 likewise approaches one-hundred percent (100%). In practice, a duty-cycle of 100% is not obtainable. However, immediately switching into a traditional boost mode algorithm from such a point is not suitable because the output voltage Vout is still less than the input voltage Vin.

Accordingly, once the output voltage Vout exceeds a second transition voltage Vt such as one diode below Vin, the present invention teaches transitioning into the pseudo-boost mode 404. The pseudo-boost mode 404 serves to facilitate a smooth transition between the pseudo-buck mode 402 and the traditional boost mode 406. Additionally, the pseudo-boost mode 404 provides even further control over the inductor current Il, thus further minimizing battery inrush current.

During an on-cycle 414 of the pseudo-boost mode 404, the gate of the NMOS switch 304 is tied to Vin, the gate of the PMOS switch 306 is tied to the greater of the input voltage Vin and the output voltage Vout, and the body of the PMOS switch 306 is tied to the output voltage Vout. As a result, during the on-cycle 414 the inductor current Il increases at a rate of Vin/L. During an off-cycle 416, the gate of the NMOS switch 304 is tied to ground 310, the gate of the PMOS switch 306 is tied to Vin, and the body of the PMOS switch 306 is tied to Lx. Thus during the off-cycle, the inductor current Il decreases at a rate of Vgs(PMOS)/L, similar to the off-cycle 412 of the pseudo-buck mode 402.

For ease of reference, the relevant control voltages for the pseudo-boost mode 404 are shown in the state diagram 400 of Figure 4, and are also provided in the following table.

Pseudo-Boost	NMOS Gate Drive	PMOS Gate Drive	PMOS Body
On-Cycle 414	Vin	Max(Vin,Vout)	Vout
Off-Cycle 416	Ground	Vin	Lx

Finally, once the output voltage exceeds the input voltage Vin, the power supply 300 will enter into a traditional boost mode, the duty-cycle control circuitry 308 implementing a suitable boost duty-cycle algorithm such as the hysterisis algorithm described above with reference to Figures 1 and 2.

Although only a few embodiments of the present invention have been described in detail herein, it should be understood that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention.

It is not essential to the present invention that the duty-cycle control circuitry implement the algorithms for all three of the linear, pseudo-buck, and pseudo-boost modes. For example, by eliminating the linear mode, the smaller NMOS switch 302 could also be eliminated. Thus the pseudo-buck and pseudo-boost modes can be implemented on traditional boost topology without additional switching devices.

Without the linear mode, however, certain precautions must be taken to avoid the breakdown of the PMOS switch 306. Perhaps the crudest solution is to simply design the PMOS switch 306 large enough to handle the stress voltage that would arise during the pseudo-buck mode. However, more elegant solutions are contemplated. In particular, rather than coupling the gate of the PMOS switch 306 to Vin during the off-cycle 412, the control circuitry 308 could drive the gate of the PMOS switch 306 to Vin/2 or some other suitable voltage value. This would, similar to the linear mode, eliminate a high stress voltage across the PMOS switch 306.

The transistor switches described above were all MOSFET technology. However, those skilled in the art will recognize that the concepts of the present invention can be implemented utilizing other suitable variable impedance devices such as bipolar transistors.

Therefore, the present examples and embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims.

Claims

I claim

1.   A method for controlling a switching power supply to generate an output voltage
Vout from an input power supply having first and second terminals and an input voltage Vin, the
second input power supply terminal being coupled to a common ground reference, the switching
power supply including a) an inductor having first and second terminals, the first inductor
terminal and the first input power supply terminal being coupled together, the inductor having an
inductance L, b) a capacitor having first and second terminals, the second capacitor terminal
being coupled to the common ground reference, c) a first switch having a gate, a drain, and a
source, the first switch operable such that a first gate bias voltage controls a flow of current
through the first switch between the first switch drain and the first switch source, the first gate
bias voltage being a voltage potential of the first switch gate over the first switch source, the
second inductor terminal and the first switch source being coupled together, the first switch
drain, the output node and the first capacitor terminal being coupled together, d) a second switch
having a gate, a drain, and a source, the second switch operable such that a second gate bias
voltage controls a flow of current through the second switch between the second switch drain and
the second switch source, the second gate bias voltage being a voltage potential of the second
switch gate over the second switch source, the second switch drain and the second inductor
terminal being coupled together, the second switch source being coupled to the common ground
reference, and e) a diode having an anode and a cathode, the method comprising the acts of:

during a pseudo-buck mode on-cycle, coupling the second switch gate to the common
ground reference, coupling the first switch gate to the common ground reference, coupling the
diode anode to Vout, and coupling the diode cathode to the second inductor terminal, whereby
the inductor current increases at a rate of about (Vin-Vout)/L; and

during a pseudo-buck mode off-cycle, coupling the second switch gate to the common
ground reference, coupling the first switch gate to a voltage suitable to choke the current flowing
through the first switch, coupling the diode anode to Vout, and coupling the diode cathode to the
second inductor terminal, whereby during the pseudo-buck mode off-cycle the inductor current
decreases at a rate of about (the first gate bias voltage)/L.

2.   A method as recited in claim 1 wherein the first switch is a PMOS transistor.

3.   A method as recited in claim 2 wherein the diode is that diode connection formed by coupling the body of the PMOS transistor to the second inductor terminal.

4.   A method as recited in claim 1 wherein the first switch is a pnp bipolar transistor.

5.   A method as recited in claim 1 wherein the second switch is an NMOS transistor.

6.   A method as recited in claim 1 wherein the second switch is a npn bipolar transistor.

7.   A method as recited in claim 1 further comprising the acts of:

during a pseudo-boost mode on-cycle, coupling the first switch gate to the greater of Vin and Vout, coupling the second switch gates to Vin, coupling the diode anode to the second inductor terminal, and coupling the diode cathode to Vout, whereby the inductor current increases at a rate of about Vin/L; and

during a pseudo-boost mode off-cycle, coupling the second switch gate to a ground reference, coupling the first switch gate to Vin, coupling the diode anode to Vout, and coupling the diode cathode to the second inductor terminal, whereby the inductor current decreases at a rate of about (the first gate bias voltage)/L.

8.   A method as recited in claim 7 further comprising the act of sensing Vout, and wherein the power supply is operated in the pseudo-buck mode until Vout reaches a predefined threshold value V_{t1} that is less than Vin, at which point the power supply is operated in the pseudo-boost mode.

9.   A method as recited in claim 8 wherein the power supply is operated in the pseudo-boost mode when Vout is between about V_{t1} and V_{t2}, V_{t2} being greater than or equal to Vin.

10.   A method as recited in claim 9 wherein the power supply is operated according to a traditional boost duty-cycle algorithm once Vout has exceeded about V_{t2}.

11.   A method as recited in claim 9 wherein the power supply further includes a third switch having a gate, a source, and a drain, the drain being coupled to the first inductor terminal and the source being coupled to Vout.

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12.   A method as recited in claim 11 further comprising the acts of:

during a linear mode, coupling the third switch gate to Vin, thereby directly coupling the input voltage Vin to the output voltage Vout through the third switch, and disabling both the first and second switches, thereby charging the capacitor.

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13.   A method as recited in claim 12 wherein the power supply is operated in the linear mode until the output voltage Vout reaches a precharge voltage Vpc at which point the power supply is operated in the pseudo-buck mode.

14.   A method as recited in claim 11 wherein the third switch is an NMOS transistor.

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15.   A method as recited in claim 1 wherein the power supply further includes a third switch having a gate, a source, and a drain, the drain being coupled to the first inductor terminal and the source being coupled to Vout.

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16.   A method as recited in claim 15 further comprising the acts of:

during a linear mode, coupling the third switch gate to Vin, thereby directly coupling the input voltage Vin to the output voltage Vout through the third switch, and disabling both the first and second switches, thereby charging the capacitor.

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17.   A method as recited in claim 16 wherein the power supply is operated in the linear mode until the output voltage Vout reaches a precharge voltage Vpc at which point the power supply is operated in the pseudo-buck mode.

18.   A method as recited in claim 15 wherein the third switch is an NMOS transistor.

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19.   A method as recited in claim 1 wherein the voltage suitable to choke the current flowing through the first transistor is set to the input voltage Vin.

20.   A method as recited in claim 1 wherein the voltage suitable to choke the current flowing through the first transistor is set to a fraction of the input voltage Vin.

21.   A method as recited in claim 20 wherein the fraction of the input voltage Vin is Vin/2.

22.   A method for controlling a switching power supply to generate an output voltage Vout from an input power supply having first and second terminals and an input voltage Vin, the second input power supply terminal being coupled to a common ground reference, the switching power supply including a) an inductor having first and second terminals, the first inductor terminal and the first input power supply terminal being coupled together, the inductor having an inductance L, b) a capacitor having first and second terminals, the second capacitor terminal being coupled to the common ground reference, c) a first switch having a gate, a drain, and a source, the first switch operable such that a first gate bias voltage controls a flow of current through the first switch between the first switch drain and the first switch source, the first gate bias voltage being a voltage potential of the first switch gate over the first switch source, the second inductor terminal and the first switch source being coupled together, the first switch drain, the output node and the first capacitor terminal being coupled together, d) a second switch having a gate, a drain, and a source, the second switch operable such that a second gate bias voltage controls a flow of current through the second switch between the second switch drain and the second switch source, the second gate bias voltage being a voltage potential of the second switch gate over the second switch source, the second switch drain and the second inductor terminal being coupled together, the second switch source being coupled to the common ground reference, and e) a diode having an anode and a cathode, the method comprising the acts of:

during a pseudo-boost mode on-cycle, coupling the first switch gate to the greater of Vin and Vout, coupling the second switch gate to Vin, coupling the diode anode to the second inductor terminal, and coupling the diode cathode to Vout, whereby the inductor current increases at a rate of about Vin/L; and

during a pseudo-boost mode off-cycle, coupling the second switch gate to a ground reference, coupling the first switch gate to Vin, coupling the diode anode to Vout, and coupling the diode cathode to the second inductor terminal, whereby the inductor current decreases at a rate of about (the first gate bias voltage)/L.

23.   A method as recited in claim 22 wherein the first switch is a PMOS transistor.

24.   A method as recited in claim 23 wherein the diode is that diode formed in the body of the PMOS transistor.

25.   A method as recited in claim 22 wherein the first switch is a pnp bipolar transistor.

26.   A method as recited in claim 22 wherein the second switch is an NMOS transistor.

27.   A method as recited in claim 22 wherein the second switch is a npn bipolar transistor.

28.   A method as recited in claim 22 further comprising the act of sensing Vout, and wherein the power supply is operated in the pseudo-boost mode until Vout reaches a predefined threshold value V_o that is greater than or equal to Vin, at which point the power supply is operated according to a traditional boost duty-cycle algorithm.

29.   A method as recited in claim 28 wherein the power supply further includes a third switch having a gate, a source, and a drain, the drain being coupled to the first inductor terminal and the source being coupled to Vout, the method further comprising the act of:
        operating in a linear mode until the output voltage Vout reaches a precharge voltage Vpc, wherein during the linear mode the third switch gate is coupled to Vin, and both the first and second switches are disabled, thereby directly coupling the input voltage Vin to the output voltage Vout and charging the capacitor.

30.   A method as recited in claim 29 wherein the third switch is an NMOS transistor.

31.   A method for controlling a switching power supply to generate an output voltage Vout from an input power supply having first and second terminals and an input voltage Vin, the second input power supply terminal being coupled to a common ground reference, the switching power supply including a) an inductor having first and second terminals, the first inductor terminal and the first input power supply terminal being coupled together, the inductor having an inductance L, b) a capacitor having first and second terminals, the second capacitor terminal

being coupled to the common ground reference, c) a first switch having a gate, a drain, and a source, the first switch operable such that a first gate bias voltage controls a flow of current through the first switch between the first switch drain and the first switch source, the first gate bias voltage being a voltage potential of the first switch gate over the first switch source, the second inductor terminal and the first switch source being coupled together, the first switch drain, the output node and the first capacitor terminal being coupled together, d) a second switch having a gate, a drain, and a source, the second switch operable such that a second gate bias voltage controls a flow of current through the second switch between the second switch drain and the second switch source, the second gate bias voltage being a voltage potential of the second switch gate over the second switch source, the second switch drain and the second inductor terminal being coupled together, the second switch source being coupled to the common ground reference, e) a third switch having a gate, a source, and a drain, the drain being coupled to the first inductor terminal and the source being coupled to Vout and f) a diode having an anode and a cathode, the method comprising the acts of:

operating in a linear mode until the output voltage Vout reaches a precharge voltage Vpc, wherein the third switch gate is coupled to Vin, and both the first and second switches are disabled, thereby directly coupling the input voltage Vin to the output voltage Vout and charging the capacitor;

operating in a pseudo-buck mode when the output voltage Vout is between about Vpc and a first threshold voltage V_{t1}, the pseudo-buck mode having:

a pseudo-buck mode on-cycle wherein the first and second switch gates are coupled to the common ground reference, the diode anode is coupled to Vout, and the diode cathode is coupled to the second inductor terminal; and

a pseudo-buck mode off-cycle wherein the second switch gate is coupled to the common ground reference, the first switch gate is coupled to the input voltage Vin, the diode anode is coupled to Vout, and the diode cathode is coupled to the second inductor terminal; and

operating in a pseudo-boost mode when the output voltage exceeds the first threshold voltage V_{t1}, the pseudo-boost mode having:

a pseudo-boost mode on-cycle wherein the first switch gate is coupled to the greater of Vin and Vout, the second switch gate is coupled to Vin, the diode anode is coupled to the second inductor terminal, and the diode cathode is coupled to Vout; and

a pseudo-boost mode off-cycle wherein the second switch gate is coupled to the ground reference, the first switch gate is coupled to Vin, the diode anode is coupled to Vout, and the diode cathode is coupled to the second inductor terminal.

32.   A method as recited in claim 31 further comprising the act of operating according to a traditional boost duty-cycle algorithm once the output voltage Vout has exceeded a second threshold voltage V_{c2} that is greater than or equal to Vin.

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33.   A method as recited in claim 31 wherein the first switch is a PMOS transistor.

34.   A method as recited in claim 31 wherein the first switch is a pnp bipolar transistor.

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35.   A method as recited in claim 31 wherein the second switch is an NMOS transistor.

36.   A method as recited in claim 31 wherein the second switch is a npn bipolar
15   transistor.

37.   A method as recited in claim 31 wherein the third switch is an NMOS switch.

38.   A method as recited in claim 31 wherein the third switch is a npn bipolar
20   transistor.

39.   A switching power supply operable to generate an output voltage Vout from an input power supply having first and second terminals and an input voltage Vin, the second input power supply terminal being coupled to a common ground reference, the switching power supply
25   including:

an inductor having first and second terminals, the first inductor terminal and the first input power supply terminal being coupled together;

an output capacitor having first and second terminals, the second capacitor terminal being coupled to the common ground reference, the output voltage Vout being the voltage difference
30   between the first capacitor terminal and the common ground reference;

a first variable impedance device coupling the second inductor terminal and the first capacitor terminal together;

a second variable impedance device coupling the second inductor terminal and the common ground reference together; and

a control circuit capable of controlling the first variable impedance device, the second variable impedance device, and the diode, the control circuit operable to implement a pseudo-buck mode suitable for operation when the output voltage Vout is less than the input voltage Vin, wherein:

5   during a pseudo-buck mode on-cycle, the first variable impedance device and the second variable impedance device are adjusted such that all the inductor current flows through the first variable impedance device and charges the output capacitor, the first variable impedance device adjusted such that the inductor current is increasing; and

during a pseudo-buck mode off-cycle. the first variable impedance device and the second 10   variable impedance device are adjusted such that all the inductor current flows through the first variable impedance device and charges the output capacitor, the first variable impedance device adjusted such that the inductor current is decreasing.

40.   A switching power supply as recited in claim 39, wherein the rate of increase of 15   the inductor current during the pseudo-buck mode on-cycle is proportional to a difference between the input voltage Vin and the output voltage Vout.

41.   A switching power supply as recited in claim 40 wherein the rate of increase of the inductor current during the pseudo-buck mode on-cycle is about (Vin-Vout)/L. where L is the 20   inductance of the inductor.

42.   A switching power supply as recited in claim 39 wherein the rate of decrease of the inductor current during the pseudo-buck mode off-cycle is proportional to a voltage differential between the input voltage Vin and a voltage present at the second inductor terminal.
25

43.   A switching power supply as recited in claim 39 wherein the control circuit is further operable to implement a pseudo-boost mode suitable for providing a smooth transition of the output voltage Vout from a voltage less than the input voltage Vin to a voltage greater than or equal to the input voltage Vin. wherein:

30   during a pseudo-boost mode on-cycle. the first variable impedance device and the second variable impedance device are adjusted such that the inductor current is increasing and all the inductor current flows through the second variable impedance device to ground; and

during a pseudo-boost mode off-cycle. the first variable impedance device and the second variable impedance device are adjusted such that all the inductor current flows through the first

variable impedance device and charges the output capacitor, the first variable impedance device adjusted such that the inductor current is decreasing.

44.   A switching power supply as recited in claim 43 wherein a rate of increase of the inductor current during the pseudo-boost mode on-cycle is proportional to the input voltage Vin.

45.   A switching power supply as recited in claim 44 wherein the rate of increase of the inductor current is equal to Vin/L, where L is the inductance of the inductor.

46.   A switching power supply as recited in claim 43 wherein the rate of decrease of the inductor current during the pseudo-boost mode off-cycle is proportional to a voltage differential between the input voltage Vin and a voltage present at the second inductor terminal.

47.   A switching power supply as recited in claim 39 further including a third variable impedance device coupling the first inductor terminal to the first capacitor terminal.

48.   A switching power supply as recited in claim 47 wherein the third variable impedance device is an NMOS transistor.

49.   A switching power supply as recited in claim 47 wherein the third variable impedance device is a bipolar npn transistor.

50.   A switching power supply as recited in claim 48 wherein the control circuit is further capable of controlling the third variable impedance device. the control circuit operable to implement a linear mode suitable for charging the output capacitor to a precharge voltage, the linear mode adjusting the first and second variable impedance devices to their highest impedance level, and adjusting the third variable impedance device to its lowest impedance level, thereby coupling the input voltage Vin to the output voltage Vout and charging the output capacitor.

51.   A switching power supply as recited in claim 39 wherein the first variable impedance device is a PMOS transistor.

52.   A switching power supply as recited in claim 39 wherein the first variable impedance device is a bipolar pnp transistor.

53. A switching power supply as recited in claim 39 wherein the second variable impedance device is an NMOS transistor.

5   54.   A switching power supply as recited in claim 39 wherein the second variable impedance device is a bipolar npn transistor.

55.   A switching power supply as recited in claim 39 wherein the control circuit includes a microprocessor.

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56.   A switching power supply as recited in claim 39 wherein the control circuit includes programmable logic.

57.   A switching power supply as recited in claim 39 wherein the control circuit

15   includes an application specific integrated circuit (ASIC).

58.   A switching power supply as recited in claim 39 wherein each element is formed within a single integrated circuit package.
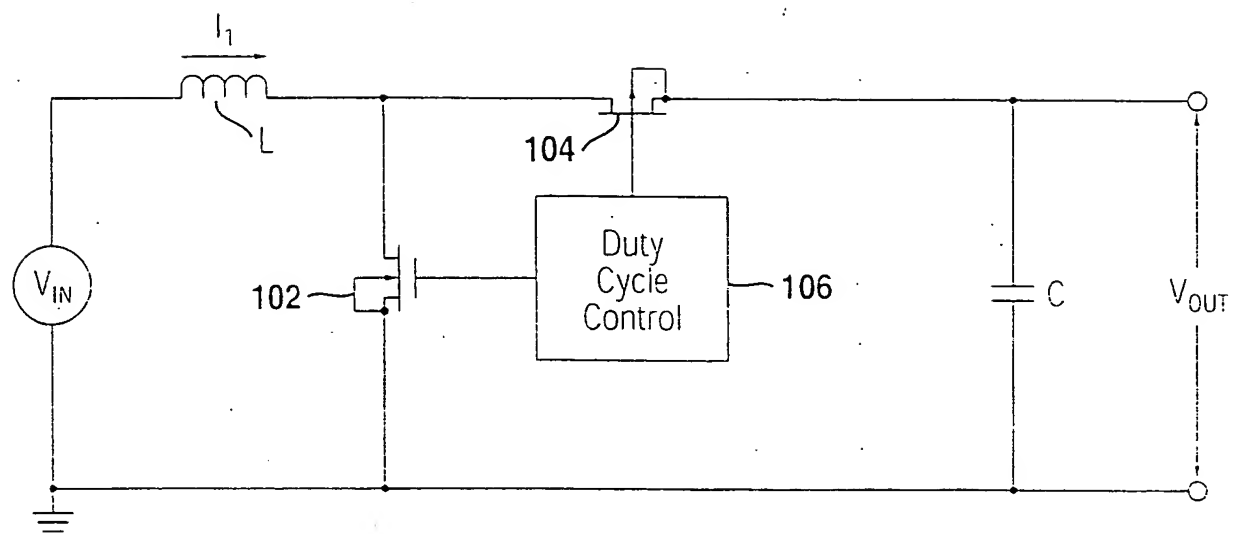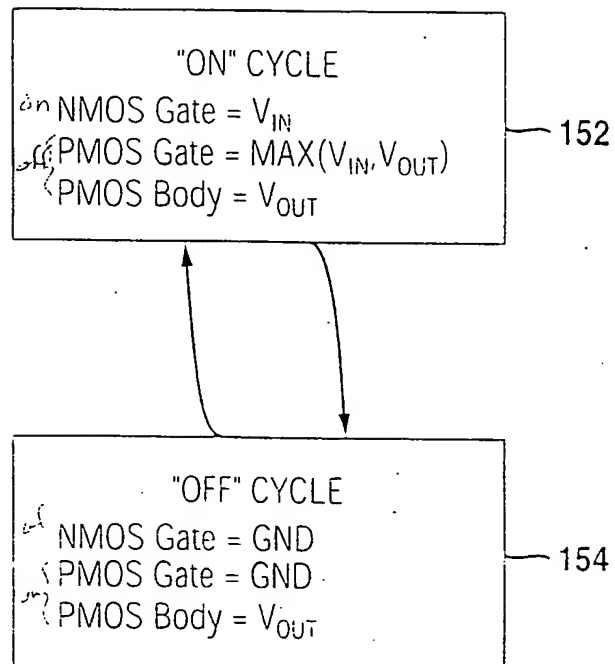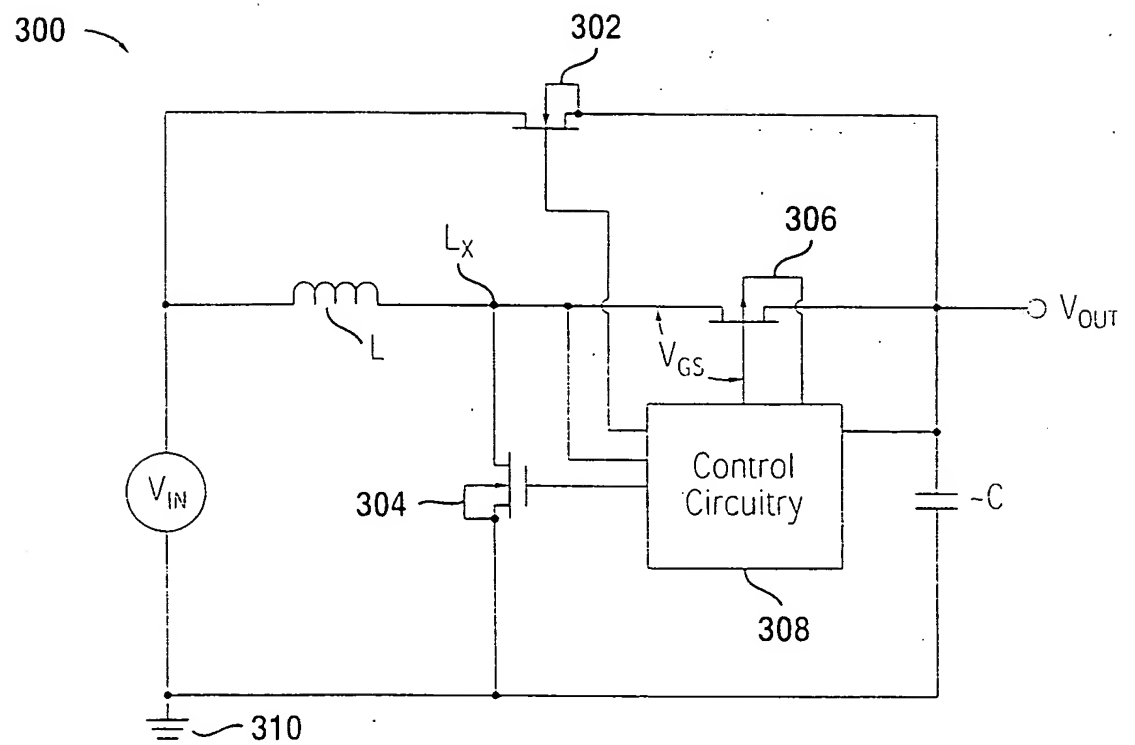
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Fig. 1
(Prior Art)

150 ⌐


```
          ┌─────────────────────────────────────┐
          │            "ON" CYCLE               │
          │  NMOS Gate = V_IN                   │── 152
          │  PMOS Gate = MAX(V_IN, V_OUT)       │
          │  PMOS Body = V_OUT                  │
          └─────────────────────────────────────┘
                          ↕
          ┌─────────────────────────────────────┐
          │            "OFF" CYCLE              │
          │  NMOS Gate = GND                    │── 154
          │  PMOS Gate = GND                    │
          │  PMOS Body = V_OUT                  │
          └─────────────────────────────────────┘
```

"ON" CYCLE

NMOS Gate = V_{IN}

PMOS Gate = $MAX(V_{IN}, V_{OUT})$

PMOS Body = V_{OUT}

— 152

"OFF" CYCLE

NMOS Gate = GND

PMOS Gate = GND

PMOS Body = V_{OUT}

— 154

Fig. 2
(Prior Art)

Fig. 3

406 BOOST MODE

414 → **"ON" CYCLE**
NMOS Gate = V_{IN}
PMOS Gate = MAX(V_{IN}, V_{OUT})
PMOS Body = V_{OUT}

"OFF" CYCLE
NMOS Gate = GND
PMOS Gate = GND
PMOS Body = V_{OUT}

404 PSEUDO-BOOST MODE

414 **"ON" CYCLE**
NMOS Gate = V_{IN}
PMOS Gate = MAX(V_{IN}, V_{OUT})
PMOS Body = V_{OUT}

416 **"OFF" CYCLE**
NMOS Gate = GND
PMOS Gate = V_{IN}
PMOS Body = L_{X2}

V_{OUT} V_{PC}

402 PSEUDO-BUCK MODE

410 **"ON" CYCLE**
NMOS Gate = GND
PMOS Gate = GND
PMOS Body = L_{X2}

412 **"OFF" CYCLE**
NMOS Gate = GND
PMOS. Gate = V_{IN}
PMOS Body = L_{X2}

400

Fig. 4

A.	CLASSIFICATION OF SUBJECT MATTER

IPC(6) :Please See Extra Sheet.
US CL :Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B.	FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

 U.S. : 323/272, 908, 276, 268, 271, 272, 273, 274, 275, 276, 222; 363/49, 50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
 NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
 US PTO APS

C.	DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,144,222 A (HERBERT) 01 September 1992, (01.09.92), see abstract and column 2.	1-58
A	US 5,313,382 A (FARRINGTON) 17 May 1994, (17.05.94) see abstract, see figures 1, 14, 15 and column 2, lines 7-24.	1-58
A	US 5,402,060 A (ERISHMAN) 28 March 1995, (28.03.95), see abstract, see figures and column 3, lines 39-68, column 4, lines 1-14.	1-58
A	US 5,565,761 A (HWANG) 15 October 1996, (15.10.96), see abstract and figures 11 and 12.	1-58
A	US 5,602,463 A (BENDALL et al) 11 February 1997, (11.02.97), see figures 1 and 4, and abstract.	1-58

[X]	Further documents are listed in the continuation of Box C.	[ ]	See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)		
"O"	document referring to an oral disclosure, use, exhibition or other means	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 JULY 1999	04 AUG 1999

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	BAO VU
Facsimile No. (703) 305-3230	Telephone No. (703) 308-2318

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,736,842 A (JOVANOVIC) 07 April 1998, (07.04.98), see abstract, figures and column 4.	1-58
A, P	US 5,856,919 A (MORIARTY, JR.) 05 January 1999, (05.01.99), see figure 1 and abstract and column 2.	1-58

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (6):

G05F 1/40, 1/569; H02H 7/10

A. CLASSIFICATION OF SUBJECT MATTER:
US CL :

323/272, 908, 276, 268, 271, 272, 273, 274, 275, 276, 222; 363/49, 50